CLAIMS

1. An integrated circuit for a printhead, comprising:

a substrate;

a transistor formed in the substrate wherein the gate of the transistor forms at least one closed loop; and

an ejection element coupled to the transistor wherein the ejection element is disposed over the substrate without an intervening field oxide layer.

2. The integrated circuit of claim 1, further comprising a dielectric layer disposed between the ejection element and the substrate having a thickness greater than 2,000 Angstroms.

3. The integrated circuit of claim 2, wherein the dielectric layer is phosphosilicate glass.

4. The integrated circuit of claim 2, wherein the dielectric layer is comprised of a layer of thermal oxide and a layer of phosphosilicate glass.

5. The integrated circuit of claim 1 wherein the transistor has a bulk that is not directly connected to the substrate.

6. The integrated circuit of claim 1 wherein the transistor is formed without an active mask definition.

7. The integrated circuit of claim 1 wherein the transistor has a gate oxide formed with a layer of silicon dioxide and a layer of silicon nitride.

8. A printhead, comprising:

the integrated circuit of claim 1; and

an orifice layer defining a nozzle fluidically coupled to the ejection element and wherein the nozzle is further fluidically coupled to a fluid channel to deliver fluid to the ejection element.

9. A fluid cartridge, comprising:

the printhead of claim 8;

a body having a fluid reservoir fluidically coupled to the fluid channel of the printhead; and

a pressure regulator for maintaining a negative pressure relative to the ambient air pressure to prevent the fluid within the printhead from drooling out of the nozzle without activation of the ejection element.

10. A recording device, comprising:

the fluid cartridge of claim 9; and

a transport mechanism for moving the fluid cartridge in at least one direction with respect to a recording media.

11. An integrated circuit for a printhead, comprising:

a substrate;

a set of transistors, wherein all transistors on the substrate are formed with at least one closed loop structure;

a set of ejection elements disposed over the substrate without an intervening field oxide layer.

12. The integrated circuit of claim 11, further comprising a dielectric layer disposed between the ejection element and the substrate having a thickness greater than 2,000 Angstroms.

13. The integrated circuit of claim 12, wherein the dielectric layer is phosphosilicate glass.

14. The integrated circuit of claim 12, wherein the dielectric layer is comprised of a layer of thermal oxide and a layer of phosphosilicate glass.

15. The integrated circuit of claim 11 wherein the at least one transistor has a bulk that is not connected directly to the substrate.

16. The integrated circuit of claim 11 wherein the at least one transistor is formed without an active mask definition.

17. The integrated circuit of claim 11 wherein the transistor has a gate oxide formed with a layer of silicon dioxide and a layer of silicon nitride.

18. A printhead, comprising:

the integrated circuit of claim 11; and

an orifice layer defining a nozzle fluidically coupled to the ejection element and wherein the nozzle is further fluidically coupled to a fluid channel to deliver fluid to the ejection element.

19. A fluid cartridge, comprising:

the printhead of claim 18;

a body having a fluid reservoir fluidically coupled to the fluid channel of the printhead; and

a pressure regulator for maintaining a negative pressure relative to the ambient air pressure to prevent the fluid within the printhead from drooling out of the nozzle without activation of the ejection element.

20. A recording device, comprising:

the fluid cartridge of claim 19; and

a transport mechanism for moving the fluid cartridge in at least one direction with respect to a recording media.

Sub A6

21. A printhead having at least one transistor integrated thereon, the printhead comprising:

a substrate;

a transistor positioned on the substrate, the transistor comprising a source region, a drain region, and a gate positioned between the source region and the drain region, the gate forming a closed loop and comprising,

a layer of silicon dioxide disposed over the substrate, and

a layer of polycrystalline silicon directly on the layer of silicon dioxide;

a layer of dielectric material covering the substrate having a plurality of openings there through, the openings providing access the source region, the drain region, and the gate of the transistor;

a layer of electrically resistive material positioned on the layer of dielectric material and in direct electrical contact with the source region, the drain region, and the gate through the openings;

a layer of conductive material affixed to a portion of the layer of electrically resistive material in order to form a multi-layer structure , the layer of electrically resistive material having at least one uncovered section capable of functioning as an ejection element, the layer of electrically resistive material being covered with the layer of conductive material at the source region, the drain region and the gate of the transistor;

a portion of protective material positioned on the ejection element; and

an orifice layer having at least one nozzle, the orifice layer secured to the portion of protective material having a section thereof removed directly beneath the nozzle in order to form a fluid well in order to impart energy from the ejection element.

22. The printhead structure of claim 21 wherein the layer of electrically resistive material is comprised of a mixture of tantalum and aluminum.

Sub A7

23. The printhead structure of claim 21 wherein the layer of electrically resistive material is comprised of polycrystalline silicon.

24. The printhead structure of claim 21 wherein the layer of conductive material comprises a metal selected from the group consisting of aluminum, copper, and gold.

25. The printhead structure of claim 21 wherein the layer of dielectric material comprises a layer of phosphosilicate glass.

26. The printhead structure of claim 21 wherein the layer of dielectric material comprises a layer of thermal oxide.

27. The printhead structure of claim 21 wherein the transistor has a gate oxide a layer of silicon nitride disposed between the gate and substrate.

28. The printhead structure of claim 21 wherein the portion of protective material comprises:

a first passivation layer positioned on the ejection element, the first passivation layer being comprised of silicon nitride;

a second passivation layer positioned on the first passivation layer, the second passivation layer being comprised of silicon carbide;

a cavitation layer positioned on the second passivation layer, the cavitation layer being comprised of a metal selected from the group consisting of tantalum, tungsten, and molybdenum; and

a fluid barrier layer positioned on the cavitation layer, the fluid barrier layer being comprised of plastic, the orifice layer being secured to the fluid barrier layer.

29. A method of creating a integrated circuit having a combined transistor and an ejection element, consisting essentially of the steps of:

applying a first dielectric layer on a substrate to form a gate oxide;

applying a first conductive layer of closed loops to define gate regions of transistors;

applying a dopant concentration in the areas of the substrate not obstructed by the first conductive layer to create active regions of the transistor;

applying a second dielectric layer to a predetermined thickness to provide sufficient thermal isolation between the later formed ejection element and the substrate;

creating a first set of contact regions in the second dielectric layer;

applying a second conductive layer used to create the ejection element; and

applying a third conductive layer to connect the active regions of the transistor to the ejection element.

30. An integrated circuit created by the method of claim 29.

31. The method of claim 29 further comprising the step of creating a second set of contact regions in the first conductive layer and first dielectric layer.

32. A method of creating a printhead comprising the method of claim 29 and comprising the steps of:

applying a passivation layer over the previously applied layers on the substrate;

creating a second set of contact regions in the passivation layer to the third conductive layer;

applying a cavitation layer on the passivation layer; and

applying a fourth conductive layer to make contact with the third conductive layer through the second set of contact regions in the passivation layer.

33. A printhead created by the method of claim 32.

34. The method of claim 32 further comprising the step of applying an orifice layer over the previous applied stack of thin-film layers on the substrate.

35. A printhead created by the method of claim 34.

36. A method of creating an integrated circuit having a transistor and an ejection element, comprising the steps of:

not using an active mask to create active regions on a substrate;

not growing field oxide;

applying a gate oxide on the substrate;

applying a first conductive layer on the gate oxide;

using a gate mask having closed loop structures to create transistor gates in the first conductive layer;

applying a dopant concentration in the areas of the substrate not obstructed by the first conductive layer to create active regions of the transistor;

applying a dielectric layer to a predetermined thickness to provide a thermal isolation layer between the substrate and the ejection element;

using a contact mask to etch a first set of contact regions in the dielectric layer;

applying a second conductive layer having a high resistance;

applying a third conductive layer having a low resistance on the first conductive layer;

using a metal1 mask to define conductive traces and the ejection element by etching the third conductive layer;

applying a passivation layer on the substrate;

using a via mask to etch a second set of contact regions in the passivation layer;

depositing a cavitation layer on the substrate;

using a cavitation mask to pattern and etch the cavitation layer;

applying a fourth conductive layer on the substrate; and

using a metal2 mask to pattern and etch the fourth conductive layer to form conductive traces.

37. An integrated circuit created by the method of claim 36.

38. The method of claim 36 further comprising the step of forming a plurality of openings through the layer of first conductive layer and gate oxide in order to provide access to the substrate.

39. A method for manufacturing a printhead having at least one transistor integrated thereon comprising the steps of:

providing a substrate;

forming a layer of silicon dioxide on the substrate;

forming a layer of polycrystalline silicon on the layer of silicon dioxide, the layer of polycrystalline silicon and the layer of silicon dioxide thereunder together forming a gate of the transistor wherein the gate has a closed loop structure;

forming a transistor source region and a transistor drain region within the substrate adjacent the gate;

applying a layer of dielectric material onto the silicon dioxide layer, the gate, the source region, and the drain region;

forming a plurality of openings through the layer of dielectric material in order to provide access to the gate, the source region, and the drain region;

applying a layer of electrically resistive material onto the layer of dielectric material, the layer of electrically resistive material being in direct electrical contact with the gate, the source region, and the drain region through the openings;

applying a layer of conductive material onto the layer of electrically resistive material in order to form a multi-layer structure, the layer of electrically resistive material in the multi-layer structure having at least one uncovered section wherein the layer of conductive material is absent therefrom, the uncovered section functioning as an ejection element, the layer of electrically resistive material being covered with the layer of conductive material at the source region, the drain region, and the gate of the transistor;

applying a portion of protective material onto the resistor; and

securing an orifice layer having at least one nozzle therethrough onto the portion of protective material, the portion of protective material having a section thereof removed directly beneath the opening through the orifice layer in order to form a fluid well thereunder, the ejection element being positioned beneath and in alignment with the fluid well in order to impart energy thereto.

40. A printhead created by the method of claim 39.

41. The method of claim 39 wherein the layer of electrically resistive material is comprised of a mixture of tantalum and aluminum.

42. The method of claim 39 wherein the layer of electrically resistive material is comprised of polycrystalline silicon.

43. The method of claim 39 further comprising the step of forming a plurality of openings through the layer of first conductive layer and gate oxide in order to provide access to the substrate.

44. The method of claim 39 wherein the applying of the portion of protective material comprises the steps of:

applying a first passivation layer comprised of silicon nitride onto the resistor;

applying a second passivation layer comprised of silicon carbide onto the first passivation layer;

applying a cavitation layer comprised of a metal selected from the group consisting of tantalum, tungsten, and molybdenum onto the second passivation layer; and

applying a fluid barrier layer comprised of plastic onto the cavitation layer, the orifice layer being secured to the fluid barrier layer.

45. A printhead created by the method of claim 44.